pending claims. The MPEP (section 2144.03,2100-129), the rationale supporting an obviousness rejection may be based on common knowledge in the art or "well-known" prior art. The Examiner may take official notice of facts outside of the record which are capable of instant and unquestionable demonstration as being "well-know" in the art. If the applicant traverses such an assertion the Examiner should cite a reference in support of his or her position. **The applicant traverses the Examiner's position, as will be explained as follows, and respectfully requests the Examiner to cite reference(s) in support of his position so that the applicant can properly respond to the Examiner's rejection.**

The Examiner has further stated, "the arrangement of parts (processors, memory, etc.) is considered to be an obvious arrangement of parts well within the capabilities of one skilled in the art when taken in combination with Weiss" MPEP (2143:2100-124) states, "a statement that modifications of the prior art to meet the claimed invention would have been well within the ordinary skill in the art at the time the claimed invention was made because the relied upon references teach that all aspects of the claimed invention were individual known in the art is not sufficient to establish a prima facie case of obviousness without some objective without some objective reason to combine the teachings of the references." The applicant asserts, as will be described below, that the Examiner does not provide an objective reason for the drastic modifications to Weiss, which he proposes

In the office action dated March 26, 2002, examiner states, "with respect to claims 16 and 17 the specific use of a PCI expansion card where the bus is a PCI bus will not be given any patentable weight since there is no inherent benefit evidenced by the recitation in claim 1 that a plurality of different bus and interconnectivity standards may be used." Claim 10 from which claim 16 depends was amended after the examiner's response to recite, "a mother board, said motherboard comprising ...one or more buses on the more on the motherboard wherein each of the one or more buses uses an interface protocol selected from a group consisting of peripheral component interconnect (PCI), industrial standard architecture (ISA), Versa Module Europa (VME), and accelerated graphics port (AGP);" and "one or more expansion slots for connecting a board to the buses" ..... "a gaming processing subsystem designed to control a game played on the gaming machine, the gaming processing subsystem comprising, a first gaming processing subsystem board connected to one of the buses on the motherboard, the first gaming processing subsystem board comprising"..... "a bus interface for connecting the first gaming processing subsystem board to one of the buses via one of the expansion slots on the motherboard." Claim 16 reads, "wherein the gaming processor subsystem board is a PCI expansion card designed to interface with a PCI bus." **Thus, in the present invention, the gaming processing subsystem may be embodied on a PCI expansion card (cards compatible with other types of buses may also be used) that is designed to be plugged into an expansion slot on a motherboard of a common PC-type computing system.** In the specification of the present invention, it states, "preferably, the general computing platform or subsystem consists of a common PC-type

personal computer and therefore preferably consists of a PCI type expansion card that includes bus interface 14."

Applicant believes a gaming processing subsystem board embodied on a card that can be plugged into an expansion slot on a motherboard is a patentable distinct limitation over what is taught in Weiss that the examiner has not considered. In embodiments of the present invention, the card may be a full-length (~12 inches long) or a half length (~8 inches long) PCI card. Weiss teaches in Cols. 11 and 12 and FIG. 6, a secure processing area in use and operation including a processor board, a main board, a back plane, a graphics systems processor, memory, communications handler (additional elements are also described). If it is the examiner's assertion that the incorporation of all of these elements onto a card, such as a full length or half length PCI card as small as 8 inches, that can be plugged into an expansion slot on a motherboard is "Hornbook engineering" then the applicant asks the examiner to cite a reference(s) in support of his position as required by the MPEP. Applicants believe that the modifications suggested by the examiner are non-obvious and are not "Hornbook engineering," and thus, the present invention is not rendered obvious in view of Weiss.

Examiner makes the argument that since Weiss specifies a need for an open architecture design and a secure processor design, "it would have been obvious to one of ordinary skill in the art at the time of the invention to use the teaching of Weiss to connect the various processing systems, such as by using a personal computer-based design." Applicant does not follow how this logic provides a motivation for the modifications suggested by the Examiner in particular in light of what Weiss teaches. Weiss teaches a secure processing area including a processor board, a main board, a back plane, graphics systems processor, memory and communications handler. Weiss teaches a white box (unsecured processing area) that is connected to the secure processing area via a serial (RS-232) or parallel interface. The connection between white box and secure processing area is like a peripheral connection used for a printer. Weiss states the white box can be an interactive multi-media computer (see FIG.7) including a video memory card, processor board, serial/parallel card, RAM, communications handler, network interface, peripheral drivers, etc. Applicant believes the processor board in FIG. 7 is the main board or mother board in the multi-media computer. However, as is well known in the art, a multi-media computer includes a motherboard. Thus, Weiss teaches two separate systems (white box and secure processing area) with separate motherboards and with a plurality of cards connected to each motherboard. The separate systems are connected to one another via a peripheral interface, such as one used for connecting a printer. In Weiss, one system is not a board or card that plugs into a motherboard of the other system. Architecture described in the present invention as recited in claim 10 allows for a single motherboard with an expansion slot for accepting a first gaming processing subsystem board. The modifications suggested by the Examiner would require the elimination of at least one of the main boards (i.e., motherboards) in Weiss from either the secure processing area or the white box. **Applicant asks the Examiner to specify in Weiss or a prior art reference a**

motivation that justifies the elimination and consolidation of components as suggested by the Examiner. MPEP 2144.04 states, "an omission of an element with retention of the element's function is an indicia of unobviousness."

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
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APPENDIX A: Pending Claims

10. (Amended three times) A gaming machine comprising:

a housing;

a user input connected to the housing;

a display connected to the housing; and

a control system located within the housing, the control system comprising a processing platform that comprises:

a mother board, said motherboard comprising;

a first processor;

a memory wherein the first processor and the memory are designed or configured to control and operate one or more of i) visual displays, ii) attraction animation features, iii) audio player feedback, iv) real-time video presentations, v) and operating system and combinations thereof;

one or more buses on the more on the motherboard wherein each of the one or more buses uses an interface protocol selected from a group consisting of peripheral component interconnect (PCI), industrial standard architecture (ISA), Versa Module Europa (VME), and accelerated graphics port (AGP);

one or more expansion slots for connecting a board to the buses;

a gaming processing subsystem designed to control a game played on the gaming machine, the gaming processing subsystem comprising,

a first gaming processing subsystem board connected to one of the buses on the motherboard, the first gaming processing subsystem board comprising;

a second processor designed or configured to control the gaming machine and to control Input/Output to the gaming machine;

a non-volatile memory for storing at least payout information;

a data memory socket located on the first gaming processing subsystem board designed to accommodate a data prom; and

a bus interface for connecting the first gaming processing subsystem board to one of the buses via one of the expansion slots on the motherboard

wherein the first gaming processing subsystem board is designed to control one or more of: i) a game play history, ii) gaming machine access, iii) user interface devices, iv) money handling devices, v) gaming machine I/O communications, v) random number generation and vi) progressive jackpot information.

11. (Amended) The gaming machine of claim 10, further comprising:

a second gaming processing subsystem board wherein the first gaming processing subsystem board is designed to control one or more of: i) a game play history, ii) gaming machine access, iii) user interface devices, iv) money handling devices, v) gaming machine I/O communications, v) random number generation and vi) progressive jackpot information..

12. Cancelled.

13. Cancelled.

14. Cancelled.

15. The gaming machine of claim 10, further comprising:

a serial communication connection.

16. (Amended) The gaming machine of claim 10, wherein the gaming processor subsystem board is a PCI expansion card designed to interface with a PCI bus.

17. Cancelled.

18. Cancelled.

19. Cancelled.

20. The gaming machine of claim 10, wherein the processing platform employs a personal computer processor architecture.

21. (Amended) The gaming machine of claim 10, wherein the first processor on the mother board and the first gaming processing subsystem board communicate using a software driven application program interface.

22. The gaming machine of claim 10, wherein the first gaming processing subsystem board further comprises:

a serial UART (Universal Asynchronous Receiver/Transmitter).

23. The gaming machine of claim 22, wherein the serial UART is used by the first gaming processing subsystem board to communicate with internal gaming devices, external gaming devices and combinations thereof.

24. The gaming machine of claim 10, wherein the first processing subsystem board further comprises:

a random number generator.